Building Intelligent Control Systems Using Graphical System Design Software and FPGA based I/O

dipl. ing. Thorsten Mayer M.S., Manager – Strategic/Technical Marketing
National Instruments Eastern Europe
thorsten.mayer@ni.com

Abstract:

The economic downturn has forced companies across the globe to simply do more with less. In many places the missions sounded somewhat like this: Maximization of automation investment through optimization of automation processes and the reduction of energy consumption. This came along with a need for more intelligent control systems in order to operate more effectively in terms of process automation and more economically in terms of energy consumption.

The increased need for machine and process optimization requires more and more functionality such as high-speed data acquisition, integration of image processing and advanced analysis and control integrated into a unified automation platform. While conventional PLCs provide extreme reliability, they often cannot fulfill more advanced requirements in areas mentioned above. This gap is filled by PACs – Programmable Automation Controllers. PACs combine the reliability of PLCs with the computation power of a high-end PC. Over the last years we have seen many innovative products releasing in this category from various players in the market. PACs are innovation boosters by providing high-end, industrial-grade tools for data and image processing, customer control and high speed data acquisition. Graphical software tools such as NI LabVIEW, help engineers leveraging this technology to create custom solutions for any engineering task in industrial and embedded control.

This paper will introduce you to technologies, architectures and COTS (Commercial Off The Shelf Products) that provide engineers a unified tool-chain (software and hardware) for implementing PAC based systems for advanced and distributed control systems.

1 NI Reconfigurable I/O (RIO) – A high performance architecture for advanced control applications

NI reconfigurable I/O (RIO) technology is based on four components: a processor, a reconfigurable field-programmable gate array (FPGA), modular I/O hardware, and graphical design software. Combined, these components give you the ability to rapidly create custom hardware circuitry with high-performance I/O and unprecedented flexibility in system timing control.

1.1 The processor

The processor is used to deploy code to communicate with other processing units such as the FPGA, interface with peripherals, log data, and run applications. NI offers RIO systems in a variety of form factors ranging from high-performance multicore systems with symmetric multiprocessing (SMP) running the Microsoft Windows OS to small, real-time embedded systems such as NI Single-Board RIO and CompactRIO.

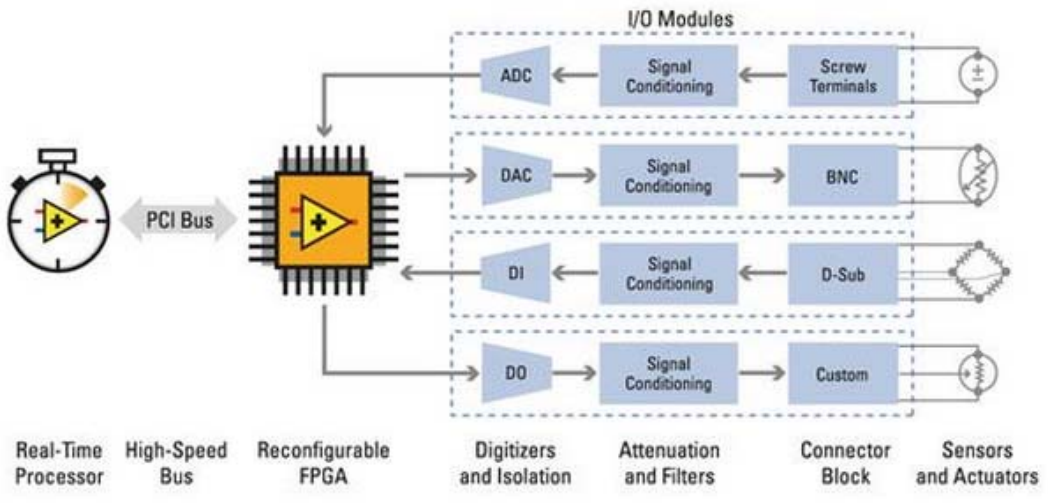

Figure 1: NI Reconfigurable I/O Architecture (RIO)

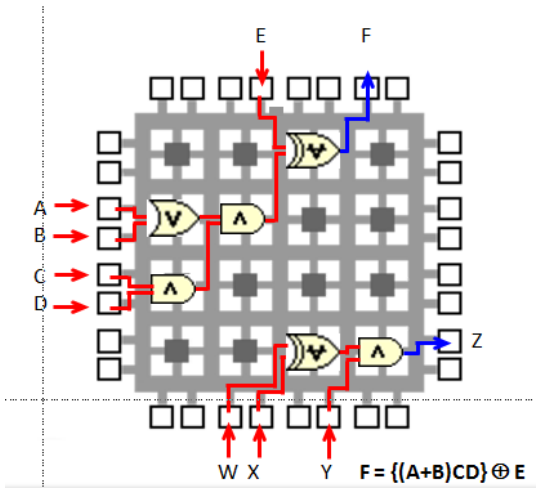

Figure 2: General FPGA architecture

1.2 The FPGA (Field Programmable Gate Array)

Fundamentally the FPGA is a piece of silicon with an ocean of transistors which are all connected together, grouped in logical blocks (ANDs, ORs, NOTs, flip-flops and memory blocks). Each of these groups can be switched programmatically. The FPGA executes programs at the speed at which the transistors propagate. This allows for the implementation of extremely fast and reliable custom control algorithms.

The reconfigurable FPGA is the core of the RIO system architecture. It is used to offload intensive tasks from the processor and provide deterministic execution with extremely high throughput. The FPGA is directly connected to the I/O modules for high-performance access to the I/O circuitry of each module and unlimited timing, triggering, and synchronization flexibility. Because each module is connected directly to the FPGA rather than through a bus, you experience almost no control latency for system response compared to other industrial controllers. Because of the FPGA speed, RIO hardware is frequently used to create controller systems that incorporate high-speed buffered I/O, very fast control loops, or custom signal filtering. For instance, using the FPGA, a single CompactRIO chassis can execute more than 20 analog proportional integral derivative (PID) control loops simultaneously at a rate of 100 kHz. Additionally, because the FPGA runs all code in hardware, it provides the high reliability and determinism that is ideal for hardware-based interlocks, custom timing and triggering, or the elimination of the custom circuitry normally required with custom sensors.

1.3 Modular I/O

NI C Series I/O modules contain isolation, conversion circuitry, signal conditioning, and built-in connectivity for direct connection to industrial sensors/actuators. By offering a variety of wiring options and integrating the connector junction box into the modules, a RIO system significantly reduces space requirements and field-wiring costs. I/O types available include ±80 mV thermocouple inputs, ±10 V simultaneous-sampling analog inputs/outputs for high speed data acquisition up to 1MS/s/channel, 24 V industrial digital I/O with up to 1 A current drive, differential/TTL digital inputs with 5 V regulated supply output for encoders, 250 Vrms universal digital inputs, industrial modules for electric power measurements, analog frame grabbers and a variety of third party modules including modules for wireless communications.

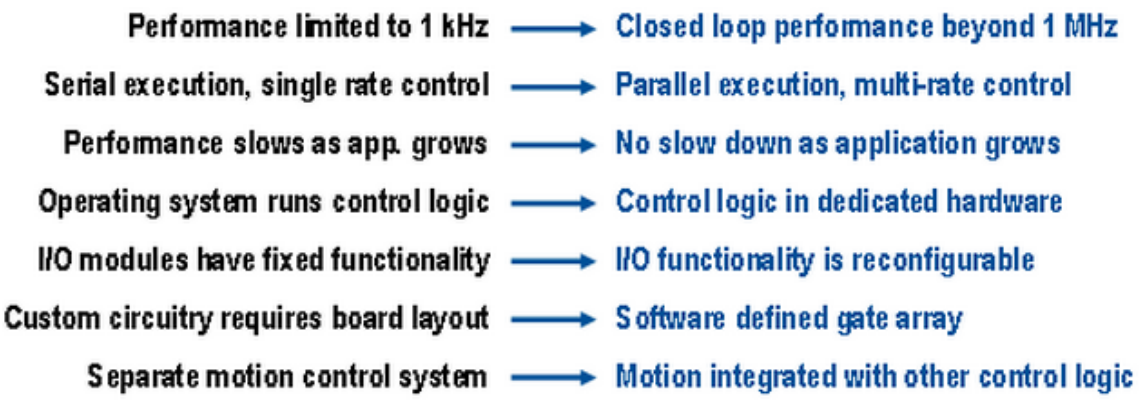

Figure 3: Micro processor based control versus FPGA based control.

1.4 Developing Applications based upon NI Reconfigurable I/O

This architecture does not come without challenges, though. Latest generation multi-core processors and FPGAs are very difficult to program. The first requires experience and parallel software development and FPGA development typically requires engineers to have hardware design experience. National Instruments has turned this architecture into a platform of commercial available products to allow any engineer and scientist to take advantage of it.

With LabVIEW graphical system design software, you can develop applications for the processor, synthesize your own custom measurement circuitry on the FPGA, and then seamlessly integrate the two with modular I/O to create a complete RIO solution.

The LabVIEW FPGA Module can help you program a field-programmable gate array (FPGA) with a LabVIEW block diagram. Under the hood, the module uses code generation techniques to synthesize the graphical development environment to FPGA hardware. This block diagram approach to FPGA is well-suited for an intuitive depiction of the inherent parallelism that FPGAs provide. Use this module with commercial off-the-shelf (COTS) hardware to create FPGA-based measurement and control hardware whether you have worked with hardware description languages (HDL) or not.

The module provides supports following specification:

- Hardware targets including both PCI/PXI boards and modular stand-alone systems.
- More than 100 FPGA IP blocks for quick development.
- Built-in I/O direct memory access (DMA) provides fast communication with a host system.
- Create logic that can execute in one cycle of 40Mhz, 80MHz, or faster clocks.
- Manage memory, FIFOs, clocks, and I/O in the LabVIEW project.
- Use available Wizards for quick-start or begin from a blank diagram.

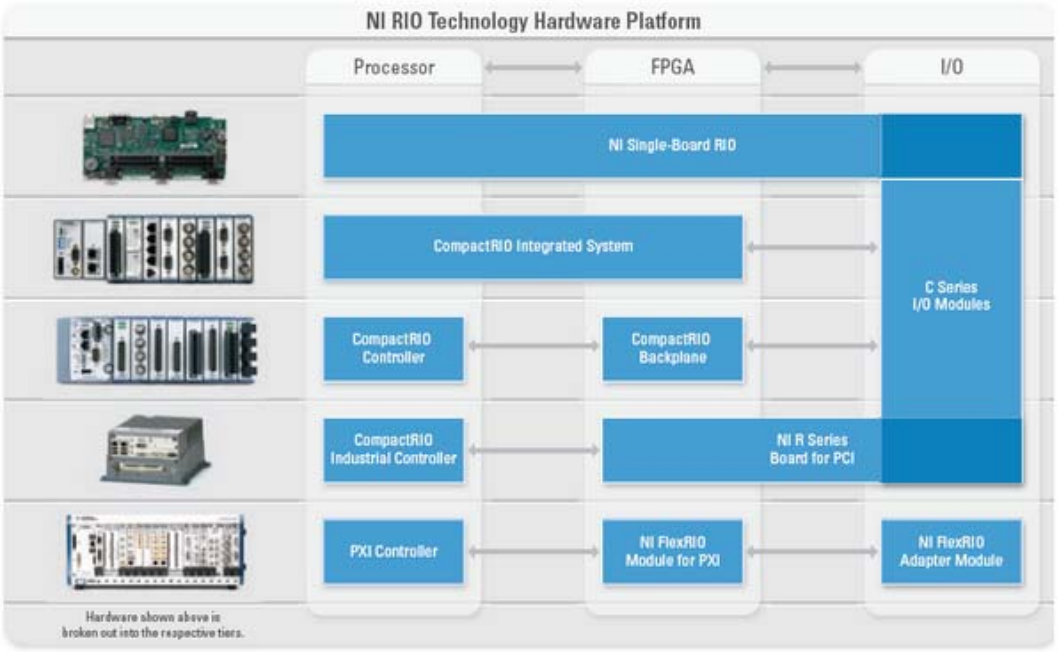

Figure 4: NI RIO technology Hardware Platform

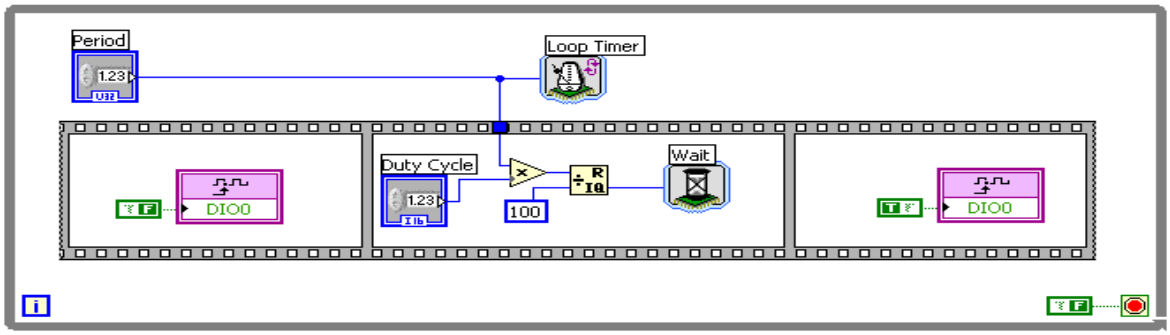

Figure 5: PWM implemented in NI LabVIEW FPGA

1.5 NI CompactRIO

CompactRIO is a small, rugged RIO system ideal for embedded and prototyping applications. Configurable with four- and eight-slot backplanes featuring a variety of FPGA options, as well as a variety of processor choices for the controller, CompactRIO offers the widest range of configuration options in the RIO family. For high-channel count systems one can take advantage of a 14-slot expansion chassis. The CompactRIO technology does also exist in form of a low-cost integrated system or for use in a truly distributed system (NI 9144 EtherCAT expansion chassis). The RIO form factors scale down to board level computers such as NI Single-Board RIO devices which integrates RIO system components (real-time processor, FPGA, and I/O) on a single board, and are designed for high-volume, embedded control and acquisition applications that require high performance and reliability.

2 Developing distributed control architectures leveraging EtherCAT and FPGA Intelligence.

The need for expansion I/O often arises when designing a real-time system with large channel counts or widespread floor space. Expansion I/O gives you the ability to add distributed measurements or expand the original application. However, building your own synchronization architecture to maintain the determinism of this control system can quickly become messy and un-scalable. Real-time Ethernet I/O technologies, such as EtherNet/IP, EtherCAT, and PROFINET, that exist today can simplify these applications, so consider using a real-time network of remote I/O that is designed to maintain deterministic communication with the main controller.

1.6 NI CompactRIO EtherCAT Slave Chassis with integrated FPGA

The NI 9144 expansion chassis adds EtherCAT I/O to your NI CompactRIO, PXI, or Industrial Controller system. This eight-slot rugged chassis for C Series modules communicates deterministically over an open, real-time Ethernet protocol called EtherCAT. You can expand your time-critical applications by daisy chaining several NI 9144 chassis from the EtherCAT master controller. Plus, the software configuration and LabVIEW programming experience are designed to be easy to use when adding real-time EtherCAT I/O.

1.7 Why add FPGA intelligence

Leveraging the FPGA of the CompactRIO Chassis will allow new levels of customization and flexibility for your control application. By embedding decision-making capabilities, it provides 100% real-time control behavior with reduced response times. The intelligent device can also offload processing from the master by conducting inline analysis, custom triggering, and signal manipulation at the node.

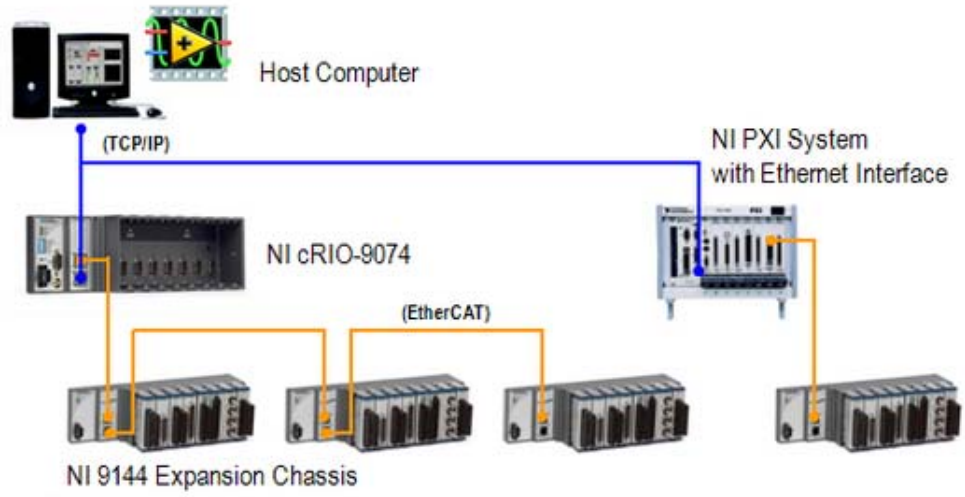

Figure 6: EtherCAT master/slave architecture with NI hardware.

1.8 Nucor Steele Corporation – A Case Study

Nucor Steel recycles steel using an electric arc furnace (EAF). Depending on the type of steel being produced, a combination of elements is added to the viscous steel to create the appropriate steel alloy. This process requires large amounts of energy that vary significantly depending on the amount of scrap placed in the furnace. One risk involved in drawing the large amount of electricity required to heat the furnace for recycling is causing flicker on the power grid. Not only did Nucor receive monetary penalties for using too much electricity, but the power grid flicker was an inconvenience to Marion residents. To reduce electricity consumption, Nucor process engineers developed an online reactor in series with the furnace using the LabVIEW FPGA module and the CompactRIO platform that measures the amount of energy drawn from the power grid. If the furnace approaches the prescribed limit, the system can quickly change control methods to reduce the amount of power being drawn. The analysis was performed in-line on the FPGA to ensure real-time response in micro seconds.

Other examples could be:

Sound intense/sensitive processes with the need to react in real-time to changing sound volumes in a distributed control environment. The master real-time code controls the plant but the slave chassis records the audio waveform measurements from a microphone and performs fast Fourier transform (FFT) on the FPGA to get the sound intensity for a specific machine or other source of sound. The slave FPGA then uses pulse width modulation (PWM) to control the sounds source in real-time without overloading the plant control system.

Rotational machinery that needs to get monitored and controlled as part of a distributed control system where deepening on noise and vibrations the machine needs to get shut down in real-time.

3 Conclusion

The increase in performance and cost of FPGAs are making these platforms truly viable to rapidly design, prototype and deploy embedded and/or industrial control systems. Because of their reliability and performance, they are ideal for highly safety critical and advanced control tasks (also read the control system for the world's largest particle accelerator - http://sine.ni.com/cs/app/doc/p/id/cs-10795). Commercial-off-the-shelf platforms and technology such as NI LabVIEW and the NI RIO hardware platform allow engineers to leverage FPGA technology to control industrial machinery and processes more effectively and economically. Using deterministic distributed I/O platforms such as the NI CompactRIO

EtherCAT expansion chassis engineers can maintain tight timing and synchronization needed for real-time applications. Plus, adding hardware-level FPGA code to EtherCAT slaves gives them the ability to offload processing from the controller and reduce response time by making intelligent decisions at the node.

4 References

[1] An Introduction to NI Reconfigurable I/O (RIO) Technology

[2] http://zone.ni.com/wv/app/doc/p/id/wv-1139/nextonly/y

[3] FPGA based Control

[4] http://zone.ni.com/devzone/cda/tut/p/id/3357

[5] Programming EtherCAT I/O with FPGA Intelligence

[6] http://zone.ni.com/devzone/cda/tut/p/id/10618#toc0

[7] Nucor Refines Steel Recycling Using NI LabVIEW and National Instruments Hardware, Dave Brandt - Nucor Corp

[8] http://sine.ni.com/cs/app/doc/p/id/cs-11227